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Analysis of LUT Faults in SRAM Based FPGA Design Using BIST

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Abstract: *FPGAs have become popular in present because of its features like high logic capacity, configurability and regular architecture with low area cost. However, FPGAs are prone to faults, testing is one of the important process for designers. Hence, the best method for testing faults in FPGAs is Built-In Self-Test (BIST). BIST is a design technique that allows a system to test itself .The proposed method of a BIST design for fault detection and fault diagnosis of Static-RAM (SRAM) based FPGAs can testLookup Tables (LUTs) in the Configurable Logic Blocks (CLBs).There are three major blocks in the system to detect and diagnose the faults. They are Test Pattern Generator (TPG), Output Response Analyser (ORA) and Block Under Test(BUT).*
Keywords: *BIST, LUT, TPG, ORA*

I. Introduction

An FPGA have been widely utilized in digital system which offer programmability at relatively less development cost and high performance [1]. An FPGA consists of logic and interconnect resources that permit to configure an uncommitted chip into the desired functions for many applications. An FPGA is a programmable logic device which consists of two dimensional array like structure ofCLBs [2]. Both CLBs and interconnect are designed with appropriate data present in the configuration memory. Static RAM (SRAM) based FPGAs consists of two types of interconnects. They are the global interconnect and local interconnect.

Local interconnects are associated with CLBs input and output pins. Local interconnect have many programmable SRAM cells compared with any other part of the routing resources. Testing an FPGA interconnect is a complex task since it takes 80% of the device area [3]. Testing methodology for detecting faults in interconnect mainly concentrate on generating many configurations for programmable SRAM cells which connect with many wire segments. Nowadays, Very Large Scale Integration (VLSI) technology keeps increasing circuit integration by ever greater degrees, and the rapid development in packaging technology greatly reduces the controllability and observability of internal nodes [4]. This significantly complicates the testing of the system. Generally, FPGAs can be configured in many ways. In BIST architecture approaches introduce both area overhead and delay penalties. The BIST approach can be applied to any in-circuit reprogrammable SRAM-based FPGAs.

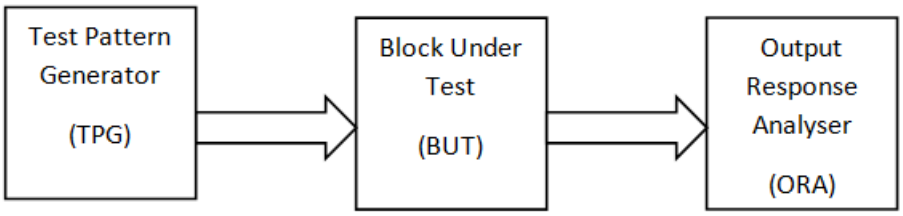

Fig 1.1 General structure for BIST test.

The main parts of BIST architecture are illustrated in Fig 1.1. TPG generates required test vectors then these vectors apply to the BUT and using ORA the final fault free outputs can be obtained.
In this paper, section II consists of related works, section III is proposed method. Section IV, is experimental Results and in section V conclusion.

II. Related Works

The scan-chains are used for pseudorandom testing in the first phase. Each stage of the Phase Shifter (PS) drives multiple scan chains, where all scan chains in the same scan tree are driven by the same stage of the PS. The scan-forest architecture is adopted to compress test data and reduce the deterministic test data volume [5]. Each scan-in signal drives multiple scan chains, as shown in Fig. 2.2, where different scan chains are

assigned for different weights. This technique can also reduce the size of the PS compared with the multiple scan-chain architecture where each stage of the PS drives one scan chain [6]. The compactor connected to the combinational part of the circuit is to reduce the size of the MISR. The size of the LFSR needed for deterministic BIST depends on the maximum number of care bits of all deterministic test vectors for most of the previous deterministic BIST methods. In some cases, the size of the LFSR can be large because of a less vectors. This may significantly increase the test data volume in order to keep the seeds [7].

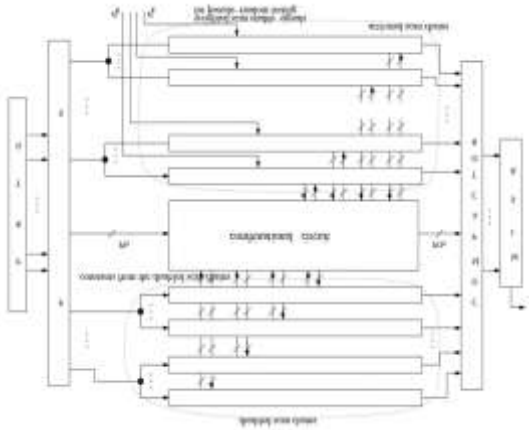

Fig 2.2 Weighted pseudorandom test generator for scan-tree-based LP BIST.

This system generates the degraded sub circuits for all subsets of scan chains in the following way. Note that all scan flip flops at the same level of the same scan tree share the same PPI [8]. For any gate, the gate is removed if its output is specified the input can be removed from a NAND, NOR, AND, and OR gates if the input is assigned a no controlling value and it has at least three inputs. For a NOR or NAND gate, the gate degrades to an inverter if one of its inputs is assigned a no controlling value [9][10].

An effective seed encoding method is used here to reduce the storage requirements for the deterministic test patterns of the random-pattern-resistant faults. A deterministic test vector is shifted into the scan trees that are activated by the gating logic, where each scan-in signal drives a number of scan trees, and only one of the scan trees driven by the same scan-in signal is activated [11]. The extra variables are introduced into the LFSR when the seed is shifted into the activated scan trees. The gating logic, partitions scan trees into multiple groups. The first group of scan trees is disabled after they have been received the test data. The second group of scan trees is activated simultaneously, and the remaining other scan trees are disabled. The seed can be stored in an extra shadow register, which is reloaded to the LFSR in a single clock cycle [12]. The scan shift operations are repeated when the extra variables are injected into the LFSR. This process continues until all scan trees have received test data.

The outputs of all scan chains, which are driven by the same clock signal, are connected to the same response compactor during the deterministic BIST phase. This offers additional flexibility in encoding [13]. The test responses of the previous test vector can be shifted out with only a few clock cycles [14]. For scan chain design, the number of clock cycles needed to shift-out test responses of the previous deterministic test vector is much larger. The proposed LP tree-based design makes the reseeding scheme much easier to implement.

III. Proposed Method

The proposed method of a LP scan based BIST design for fault detection and fault diagnosis of Static-RAM(SRAM)-based FPGAs can test both the interconnect resources [wire channels and programmable switches (PSs)] and lookup tables (LUTs) in the CLBs.The target fault detection/diagnosis of the proposed BIST structure are open/short and delay faults in the wire channels, stuck on/off faults in PSs, and stuck-at-0/1 faults in LUTs. BIST techniques in general are associated with high performance, they are also associated with high area overhead incurred by on-chip test hardware which is shown in Fig 3.3. However, the BIST overhead is not an issue for FPGA BIST because the test hardware is easily reconfigured by inserting and removing Test Pattern Generators (TPGs) and ORAs. This is particularly important for the testing of FPGAs [15].

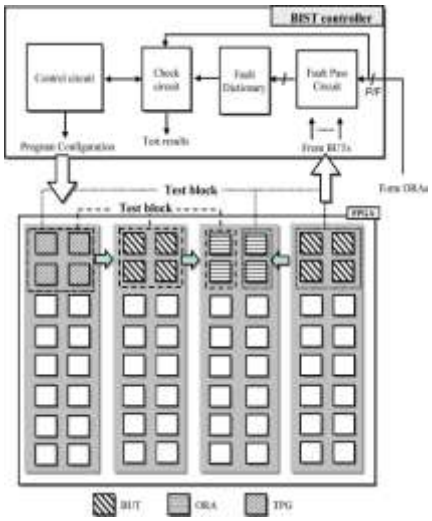

Fig 3.3 FPGA-BIST structure

In each test block, four CLBs are configured as a TPG to generate the addresses for test patterns. In addition, two CLBs are configured as an ORA for the comparison with each output of the Block Under Test (BUT) to observe the test results. The global/local interconnect resources and CLBs in a BUT, which are configured by four CLBs in a test block, are then sequentially tested. The FPGA has to be configured to shift the test blocks for eachtesting. The test processes of the proposed FPGA BIST structure are simultaneously performed by a BIST controller, which repeatedly reconfigures the test blocks for testing.

The test blocks are first configured by the BIST controller then TC considerations should be reconfigured for local interconnect resource and CLB testing. Then, the LUT-based method is used to configure the TPG and ORA to generate the test vectors. Finally, the test results are analysed.LUT based design reduces the design effort& hardware cost because new test commands can be added easily.

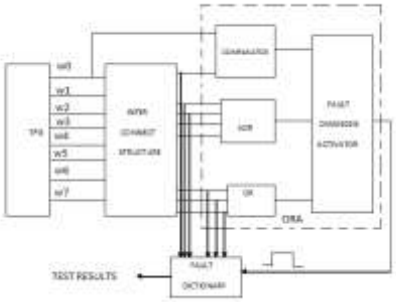

Fig 3.4 LUT structure

Test Pattern Generator(TPG):

TPG is an address generator, which consists of eight MUXs, eight LUTs, and eight DFFs .To continuously generate the addresses (0–15) in the LUTs to produce the corresponding test patterns.The LUTs addresses can be figured out in sequence with the help of MUX selection and the test patterns can be generated by repeatedly checking the contents. The four input LUT test pattern is shown in table1.

Table 1 Test pattern for a four-input LUT

Address	C1	C2	C3	C4	C5	C6	C7	C8
0000	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**
0001	**0**	**1**	**0**	**1**	**0**	**1**	**1**	**0**
0010	**0**	**1**	**0**	**1**	**1**	**0**	**0**	**1**
0011	**0**	**1**	**0**	**1**	**1**	**0**	**1**	**0**
0100	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**1**
0101	**0**	**1**	**1**	**0**	**0**	**1**	**1**	**0**
0110	**0**	**1**	**1**	**0**	**1**	**0**	**0**	**1**
0111	**0**	**1**	**1**	**0**	**1**	**0**	**1**	**0**

1000	**1**	**0**	**0**	**1**	**0**	**1**	**0**	**1**
1001	**1**	**0**	**0**	**1**	**0**	**1**	**1**	**0**
1010	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**1**
1011	**1**	**0**	**0**	**1**	**1**	**0**	**1**	**0**
1100	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**1**
1101	**1**	**0**	**1**	**0**	**0**	**1**	**1**	**0**
1110	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**1**
1111	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**

IV. Experimental Results

LUT is a simply a memory element.The fault can occur in any one of the memory element which has a single bit output either 0 or 1. Stuck-at 0 the RAM cell value of an LUT in the CLB is always 0. Stuck-at 1 fault, the RAM cell value of an LUT in the CLB is always 1.The simulation results of stuck-at 0 and stuck-at 1 are shown below.

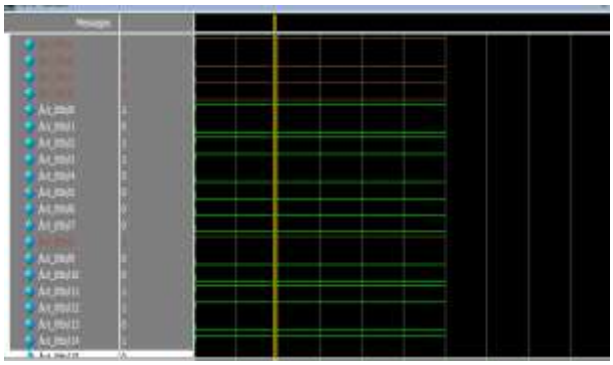

Fig 4.5 Simulation result of stuck-at 1 fault

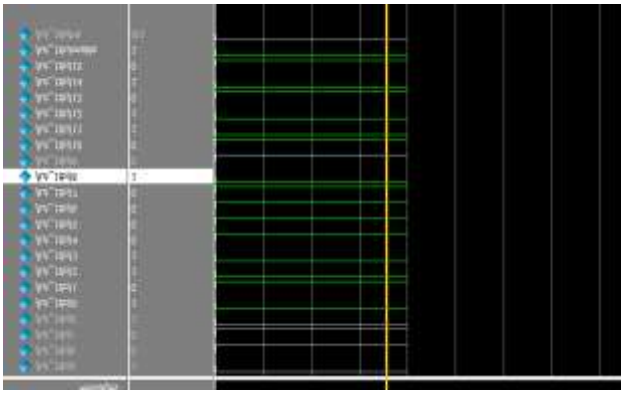

Fig 4.6 Simulation result of stuck-at 0 fault

V. Conclusion

There were two complexities faced in the existing design. They are, BSF detects each possible wire faults by the all zero vector. It is not guaranteed to identify the open faults. According to the digital system importance and by increasing the number of faults in such chips, developing efficient test methods is mandatory. In this paper SRAM- based architecture has been proposed to analyse any single stuck-at faults in the LUTs of each CLB. The faults detected in the proposed BIST structure are stuck-at 0 and stuck-at 1 faults. Hence, this paper gives a clear idea for high fault coverage in low power with SRAM based FPGA.

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